illustrates the power savings in the NMOS transistor resulting from the combination (see page 10, lines 2-3). Specifically, the application teaches that the voltage regulator can have two transistors that are driven with different gate voltages, and that both transistors can have a channel length less than that required for reliable behavior under steady state conditions. Claims 1 would read on such a voltage regulator because it has two transistors that are driven with different gate voltages. Claim 11 would also read on such a voltage regulator because it includes a transistor with a channel length less than that required for reliable behavior under steady state conditions. Since both claims would read on the voltage regulator, the inventions can be used together.

In view of the foregoing, Applicants again request that the Examiner withdraw the restriction.

II. Rejections

Claims 3-4, 8 and 18 stand rejected as indefinite. Claims 1-10 and 15-18 stand rejected as anticipated by U.S. Patent No. 5,554,561 ("Plumton").

Claims 3-4 and 18 have been amended to eliminate antecedent basis problems. With respect to claim 8, in some systems the gate of a transistor is controlled by the output of other transistors. These transistors can form a drive train. An example of a drive train is illustrated in Figure 6, although many other implementations are possible.

Claims 1 and 15 calls for a first transistor connecting the input terminal to an intermediate terminal and a second transistor connecting the intermediate terminal to ground. The first transistor includes a first gate oxide layer and the second transistor includes a second gate oxide layer. Plumpton discloses a p-channel FET 340 and a VFET 100 that are driven with different gate voltages. However, the VFET device 100 taught by Plumton does not have a gate oxide layer. In contrast to a normal CMOS device in which a gate oxide layer is disposed on a surface of the semiconductor and an applied gate voltage generates an inversion layer that turns on the device, Plumton's VFET device has gate channels formed directly in the semiconductor without any gate oxide, and the applied gate voltage creates a depletion zone that turns off the device.

As noted above, Plumton's VFET does not have a gate oxide layer. In addition, if Plumton's VFET were to be changed to a transistor that includes a gate oxide layer, the structural reason for driving the two transistor at different voltages or providing the oxide layers with different thicknesses would no longer be present. Consequently, Plumton does not teach or suggest a voltage regulator with two transistors with gate oxide layers, in which the transistors are driven with different voltages, as recited in claim 1, or in which the gates oxide layers have different thicknesses, as recited in the claim 15. Therefore, claims 1 and 15, and the claims depending therefrom, should be allowable.

Claims 19 and 20 have been amended as suggested by the Examiner.

Claims 21-24 have been added. Applicant submits that the reference to double-diffused drain structure in claim 21 does not constitute new matter. It is well known in the art that the structure illustrated in Figure 4 is called a double-diffused drain structure.

Applicant submits that the claims are in condition for allowance, which action is requested. Filed herewith is a check in payment of the excess claims fees required by the above amendments and Petition for Automatic Extension with the required fee.

Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 1/11/01

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